UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/429,297 | 10/28/1999 | Masahiko Ogino | 503.37770X00 | 5755 |

20457 7590 02/27/2003

ANTONELLI TERRY STOUT AND KRAUS
SUITE 1800
1300 NORTH SEVENTEENTH STREET
ARLINGTON, VA 22209

| EXAMINER | |
|---|---|
| MITCHELL, JAMES M | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2827 | |

DATE MAILED: 02/27/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/429,297 | OGINO ET AL. | |
| | Examiner | Art Unit | |
| | James Mitchell | 2827 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *10 December 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *2-6,9-14,17 and 20-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☒ Claim(s) *25* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

### *Drawings*

1. The drawings are objected to under 37 CFR 1.83(a) because they fail to show anisotropic conductive material for connecting circuit layer on a chip as described in the specification. Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

### *Claim Rejections - 35 USC § 103*

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 2, 3, 10, 11, 20-22 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. (U.S 6,004,467) in combination with Ball (U.S 6,351,022).

4. Kim et al. (Fig 1, 4, 5E) discloses a wafer and semiconductor device comprising a wafer (300) having a plurality of chip areas (310; Fig 4) comprising circuits and electrodes respectively and a semiconductor chip (310) that inherently possesses circuits and electrodes (shown in Fig 112) for communicating the chip with an external source, an inherent porous, stress

release, silicon dioxide layer (314; pores created by space within layer for pad) that has a breathing property on a plane, a circuit layer ("trace" 322) provided on said stress relaxing layer and connected to an electrode ("I/O pad", 312) with an external terminal (330) provided on said circuit layer, via- holes (Column 4, Lines 11-16) provided between the electrodes on said chip and said circuit layer with conductive portions for electrically connecting said circuit layer and said electrode, respective side planes of said stress relaxing layer and said chip are exposed to outside of the semiconductor device on the same plane (via singulating of chip); wherein chip is inherently mounted with other components forming a module respect.

5. Kim does not appear to disclose an organic protecting film provided on the plane opposite to said stress relaxing layer, or that the side planes of the chip, said stress relaxing layer, and an organic protecting film respectively form peripheral edges of the stress relaxing layer and are exposed to outside (understood to mean, edges free from an additional covering) of the semiconductor device on a same plane.

6. However, Ball utilizes an organic protecting film (24; Column 3, Lines 24-28)) on a front and backside of wafer.

7. It would have been obvious to one of ordinary skill in the art to form a protective film on a plane opposite to said stress relaxing layer of Kim (prior to wafer being segmented) in order to reduce breakage and cracking during handling of the structure as taught by Ball (Abstract).

8. Therefore said side planes of said stress relaxing layer, the semiconductor chip and the organic protecting film respectively would form peripheral edges of the stress relaxing and be exposed outside of the semiconductor device through a subsequent dicing process of Kim (shown in Fig 5E).

9. Claims 4, 12, 23 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. and Ball as applied to claims 2 and 10 in further view of Chang et al (U.S 6,353,182).

10. Neither Kim et al. nor Ball appear to disclose that the protecting film, stress-relaxing layer, and adhesion layer have equivalent linear coefficients.

11. However, it would have been obvious to one of ordinary skill in the art to form the protective liner, stress relaxing and adhesion layers, which are in direct contact with the chip, with equivalent linear expansion coefficients (CTE) in order to eliminate warpage in the chip due to (CTE) mismatch as evidenced by Chang et al. (Column 1, Lines 64-65).

12. Claims 5, 6 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. and Ball as applied to claims 3 and 10 in combination with Fukutake (EP 0504669).

13. Neither Kim nor Ball appears to disclose that the porous, passivating stress-relaxing layer is Polytetrafluoroethylene (PTFE).

14. However Fukutake utilizes a porous passivating PTFE layer (5; English Abstract).

15. It would have been obvious to one of ordinary skill in the art to form the porous, passivating, stress relaxing layer of the prior art with

Polytetrafluoroethylene (PTFE) in order to eliminate thermal cracking as taught by Fukutake (Abstract).

16. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. and Ball in combination with Akagawa (US 6,121,688).

17. Kim and Ball disclose the elements stated in paragraphs 4-8, but does not appear to disclose the use of ACF, however Akagawa (Fig 6) utilizes an ACF layer (38).

18. It would have been obvious to one of ordinary skill in the art to modify the interconnect of Kim by incorporating ACF in order to provide electrical connection between the chip pad and pattern as taught by Akagawa (Col. 4, Lines 21-24)

19. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kim and Ball in combination with Sasaoka (US 6,010,769).

20. Kim and Ball disclose the elements stated in paragraphs 4-8, but does not appear to disclose that a conductive portion in a via-hole is composed of a conductive resin, however Sasaoka utilizes a conductive portion (14) in a via-hole is composed of a conductive resin.

21. It would have been obvious to one of ordinary skill in the art to form the conductive structure of Kim with a conductive resin in order to form a connection as taught by Sasaoka (Col. 15, Lines 24-29).

22. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. and Ball in combination with Hasimoto (US 6,475,896).

23. Kim and Ball discloses the elements stated in paragraphs 4-8, but does not appear that the organic protective film is black, however Hasimoto utilizes an organic protective film that is black.

24. It would have been obvious to one of ordinary skill in the art to form the modified organic protective film of Kim and Ball as black, in order to increase the chip's durability to light as taught by Hashimoto (Col. 19-20, Lines 65-5)

***Allowable Subject Matter***

25. Claim 25 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

26. The following is an examiner's statement of reasons for allowance: the prior art does not disclose or make obvious that the porous stress relaxing layer has a greater porosity than that of the organic protecting film including all the limitations set forth in the independent claim.

27. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

***Response to Arguments***

28. Applicant's arguments 2-6, 10-13, and 20-24 have been considered but are unpersuasive. Applicant contends that first examiner provides no evidence that silicon dioxide provides for stress release. Second, applicant contends that a layer being porous would teach away form a passivation layer of Kim. Third

applicant contends that the protecting coatings are removed. Fourth applicant contends Chang is directed to a problem different than that of Kim and that the references are non-analogous art and that examiner provided no motivation to combine.

29. In response:

first, Roger et al (US 4,571,819) is provided to evidence that silicon dioxide provides stress relief;

second, absent a teaching of the size of the pores in relation to the material, all material is porous and therefore its small holes would not teach away from a passivation layer, because the layer would still be able to protect a surface;

third, a subsequent removal of protective coating is not germane to the issue of patentablility of the device, structurally Ball (Fig 2) discloses a point where the coating is on the device and a motivation for wanting the coating;

fourth, In response to applicant's argument that Chang is directed to a problem different than that of Kim and therefore is nonanalogous art, it has been held that a prior art reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the applicant was concerned, in order to be relied upon as a basis for rejection of the claimed invention. See *In re Oetiker*, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). In this case, Kim (Col. 1, Lines 19-31) discloses that CSP can be combined with surface mount technologies such as flip-chip, which is the same endeavor as Chang in a Flip-chip mount.

***Conclusion***

30. Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Mitchell whose telephone number is (703) 305-0244. The examiner can normally be reached on M-F 10:30-8:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Talbott can be reached on (703) 305-9883. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3432 for regular communications and (703) 305-3230 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

jmm
February 23, 2003

DAVID L. TALBOTT
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800